#### **REMARKS**

By this Amendment, Applicants add new claims 11-13, amend claims 1 and 3, and cancel claims 5-10, without prejudice or disclaimer. Therefore, claims 1-4 and 11-13 are currently pending.

### Rejection of claims 6-10 under 35 U.S.C. § 112

In a Final Office Action dated December 3, 2002, the Examiner rejected claims 6-10 under 35 U.S.C. § 112, second paragraph. By this Amendment, Applicants cancel claims 6-10, without prejudice or disclaimer. Therefore, the rejection of claims 6-10 under 35 U.S.C. § 112, second paragraph is now moot.

## Rejection of claims 1-10 under 35 U.S.C. § 103

In the Final Office Action dated December 3, 2002, the Examiner also rejected claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over <u>Ye et al.</u> (U.S. Patent No. 6,080,529) in view of <u>Lau et al.</u> (U.S. Patent No. 5,173,542). Applicants respectfully traverse this rejection.

As noted above, by this Amendment, Applicants cancel claims 5-10, without prejudice or disclaimer. Therefore, the rejection to claims 5-10 under 35 U.S.C. § 103 is now moot.

As to claim 1, Applicants respectfully submit that <u>Ye et al.</u> and <u>Lau et al.</u>, alone or in combination, fail to teach, or suggest, the features of claim 1. For example, claim 1 now recites a combination of steps including, *inter alia*, "removing the photoresist pattern and shrinking the low-dielectric pattern, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time."

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Ye et al. fails to teach such a feature. Indeed, the Examiner correctly acknowledges that Ye et al. does not teach shrinking a low dielectric pattern. (See Final Office Action at page 4.) However, the Examiner alleges that it would have been obvious to combine the teachings of Ye et al. with Lau et al. to arrive at the features of claim 1. Applicants respectfully disagree.

The Examiner asserts that <u>Lau et al.</u> teaches a curing process in which shrinkage of a low dielectric pattern occurs naturally. (See Final Office Action at page 4 and Advisory Action dated March 19, 2003 at page 2.) However, <u>Lau et al.</u> does not teach shrinking a low dielectric pattern. Instead, <u>Lau et al.</u> teaches a curing process that is designed to avoid swelling that occurs after soft baking. That is, the curing process of <u>Lau et al.</u> causes swelling in a film, and thus, the curing process must also compensate for the swelling.

For example, <u>Lau et al.</u> at col. 14, lines 23-50 teaches that a lower temperature of about 300° C is used while curing to avoid "bubbling and void formation." In another example, <u>Lau et al.</u> teaches that the effect of curing time, curing temperature, and amount of bistriazene D is controlled in order to reduce any "crazing" that results from swelling in a film. (See <u>Lau et al.</u> at col. 16, line 49 through col. 17, line 3.) Therefore, <u>Lau et al.</u> teaches a curing process that causes swelling, but then compensates for the swelling.

In contrast, as noted above, claim 1 recites, "removing the photoresist pattern and shrinking the low-dielectric pattern, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time." <u>Lau et al.</u> instead

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teaches a curing process that causes swelling and then compensates for the swelling. In other words, <u>Lau et al.</u> relates to controlling swelling (i.e., growth) in a film that is caused by the curing process. Applicants respectfully submit that controlling growth in a film, as taught by <u>Lau et al.</u>, is not the same as shrinking a low dielectric pattern, much less "removing the photoresist pattern and shrinking the low-dielectric pattern, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time," as recited in claim 1. Therefore, Applicants respectfully submit that <u>Lau et al.</u> fails to teach or suggest at least this feature of claim 1.

Accordingly, even if <u>Ye et al.</u> and <u>Lau et al.</u> were properly combinable (which they are not), the combination <u>Ye et al.</u> and <u>Lau et al.</u> would still fail to teach or suggest all of the features of claim 1. Applicants therefore request that the rejection to claim 1 and it respective dependent claims 2-4 be withdrawn. Applicants respectfully submit that claim 1 is allowable as are claims 2-4, at least by virtue of their dependence from allowable claim 1.

### New claims 11-13

Claim 11 recites a combination of steps including, *inter alia*, "shrinking the low-dielectric pattern after the removal of the photoresist pattern." As explained above, <u>Ye et al.</u> and <u>Lau et al.</u>, alone or in combination, fail to teach shrinking a low dielectric pattern, much less "shrinking the low-dielectric pattern after the removal of the photoresist pattern," as recited in claim 11. Therefore, for at least this deficiency in both <u>Ye et al.</u> and <u>Lau et al.</u>, Applicants respectfully submit that claim 11 is allowable.

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Claims 12-13 depend from claim 11, and thus, are allowable for at least the same reasons that claim 11 is allowable, as well as for their additional features. Accordingly, Applicants respectfully request the timely allowance of new claims 11-13.

#### CONCLUSION

Attached hereto is a marked-up version of the changes made to the claims by this amendment. The attached page is captioned "Version with markings to show changes made." Deletions appear as normal text surrounded by [] and additions appear as underlined text.

By:\_

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: May 5, 2003

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# VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS:

Please cancel claims 5-10, without prejudice or disclaimer, and amend claims 1 and 3, as follows:

1. (Once Amended) A method for forming gate electrodes of a semiconductor device, the method comprising:

forming a gate insulation layer over a semiconductor wafer;

forming a conductive layer over the gate insulation layer;

forming a low-dielectric layer over the conductive layer;

forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

[removing the photoresist pattern;]

[shrinking the low-dielectric pattern; and]

removing the photoresist pattern and shrinking the low-dielectric pattern,
wherein removing the photoresist pattern and shrinking the low-dielectric pattern are
performed at the same time; and

forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

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3. (Once Amended) The method of claim 1 [or 2], wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the conductive layer for the gate electrodes; and

soft-baking the low-dielectric layer at a predetermined temperature.

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